Ordering number : EN4832B

No. 4832B

Monolithic Linear IC

LA7356, LA7356M

For Use in VCR Products PAL/SECAM (MESECAM) Discrimination IC

Overview

The LA7356 and LA7356M are PAL/SECAM discrimination ICs. Since these products do not require external circuits such as ceramic filters and tank resonators, the number of external components is reduced. Thus they allow the discriminator block to be implemented in a smaller space and at a lower cost.

Functions

- Burst/CW switching
- Limit amplifier
- Frequency - phase conversion
- Phase comparator
- Comparator

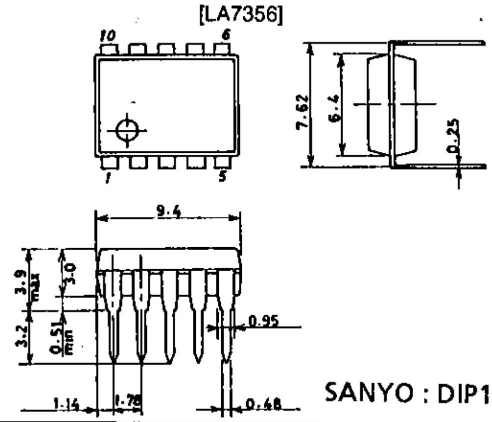
Features

- These products enable the implementation of discrimination circuits with high sensitivity even with weak signals or with strong burst input levels.
- Ceramic capacitors are the only required external components when used in conjunction with the Sanyo LA7430 and LA7435. In particular, ceramic filters and tank circuits are not required.
- Completely adjustment-free
- Low power dissipation
- Compact package

Package Dimensions

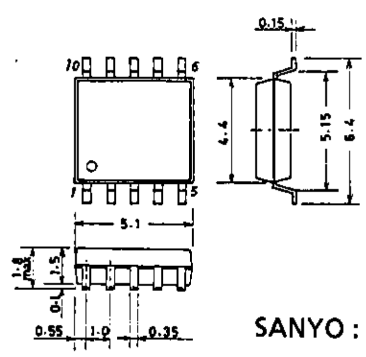
unit: mm

3098B-DIP10S



SANYO : DIP10S

3086A-MFP10S



SANYO : MFP10S

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ +65°C	120	mW
Operating temperature	Topr		–10 to +65	°C
Storage temperature	Tstg		–40 to +125	°C

Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		5.0	V
Operating supply voltage range	V_{CC} op		4.8 to 5.2	V

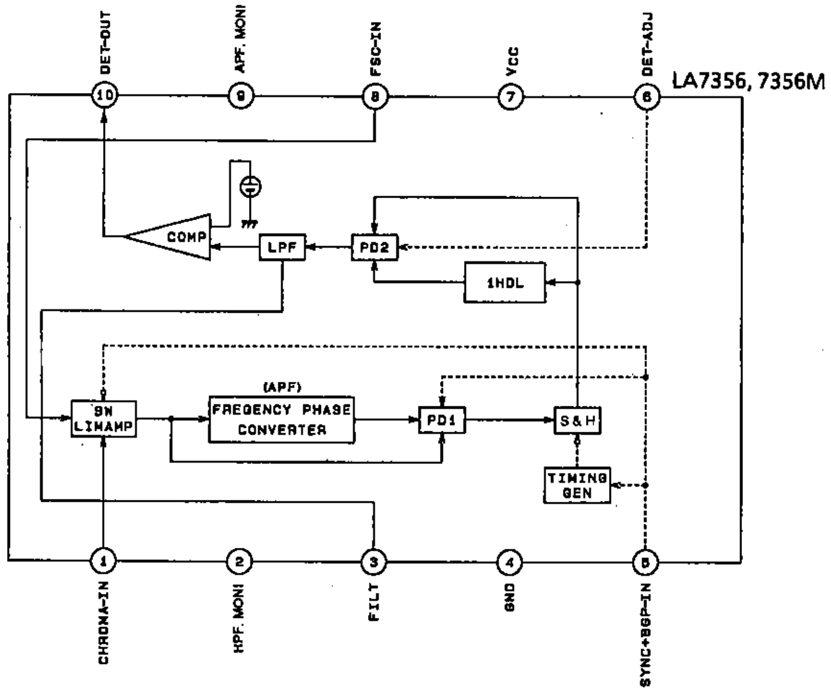
Operating Characteristics at Ta = 25°C, V_{CC} = 5 V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Quiescent current (1)	$I_{CC}1$	Pin 5 = GND, Pin 7: input current, Output: T4	7.0	10.0	13.0	mA
Quiescent current (2)	$I_{CC}2$	Pin 5 = V_{CC}, Pin 7: input current, Output: T4	7.5	10.5	13.5	mA
BGP threshold level	BTH	Slowly increase the DC voltage applied to pin 5 starting at 0 V. The pin 5 voltage input signal when a signal appears on pin 2 is 300 mV p-p. Output: T2	2.2	2.5	2.8	V
SYNC threshold level	STH	Slowly increase the DC voltage applied to pin 5 starting at 0 V. The pin 5 voltage input signal when a signal appears on pin 2 is 300 mV p-p. Output: T2	0.6	0.8	1.0	V
Input limit amplifier gain	LIMG	Defined as the output ratio when a 10 mVp-p amplitude sine wave is input to pin 1. Output: T2	9	12	15	dB
Input limit amplifier limit level	LIMD	Observe the output amplitude when a 300 mVp-p amplitude sine wave is input to pin 1. Output: T2	150	190	230	mVp-p
Comparator hysteresis voltage H	CompH	The V1 voltage when T1 goes from low to high when the voltage on V1 is gradually raised from 0 V. Output: T1	2.7	3.0	3.3	V
Comparator hysteresis voltage L	CompL	The V1 voltage when T1 goes from high to low when the voltage on V1 is gradually lowered from 5 V. Output: T1	2.0	2.3	2.6	V
DET-OUT output voltage (H)	DETH	With a 2 kΩ load resistance. Output: T1	3.6	4.0	4.4	V
DET-OUT output voltage (L)	DETL	With a 2 kΩ load resistance. Output: T1	0	0.2	0.4	V

Switch Conditions

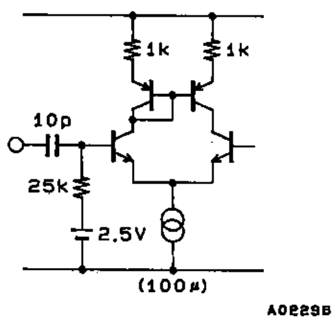
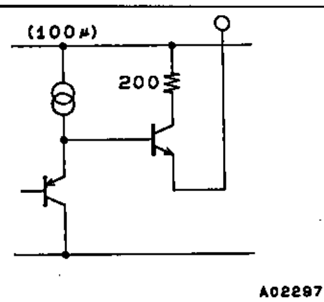
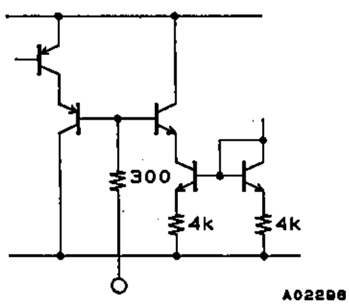
Symbol	Input signal		Input pulse		Applied voltage		Switch				
	S1	S2	S3	S4	V1	V2	SW1	SW2	SW3	SW4	SW5
$I_{CC}1$	No signal	No signal	0 V	0 V			OFF	OFF	OFF	OFF	OFF
$I_{CC}2$	No signal	No signal	5 V	5 V			OFF	OFF	OFF	OFF	OFF
BTH	Sig. 1	No signal	0 V	0 V		DC, variable	ON	OFF	ON	OFF	OFF
STH	No signal	Sig. 1	0 V	0 V		DC, variable	ON	OFF	ON	OFF	OFF
LIMG	Sig. 1	No signal	5 V	0 V			ON	OFF	OFF	OFF	OFF
LIMD	Sig. 1	No signal	5 V	0 V			ON	OFF	OFF	OFF	ON
Comp H	No signal	No signal	No signal	No signal	DC, variable		OFF	ON	OFF	OFF	ON
Comp L	No signal	No signal	No signal	No signal	DC, variable		OFF	ON	OFF	OFF	ON
DET H	Sig. 2	Sig. 1	P2	P1			OFF	OFF	OFF	OFF	ON
DET L	Sig. 3	Sig. 1	P2	P1			OFF	OFF	OFF	OFF	ON

Pin Assignment and Equivalent Circuit Block Diagram



Pin Functions

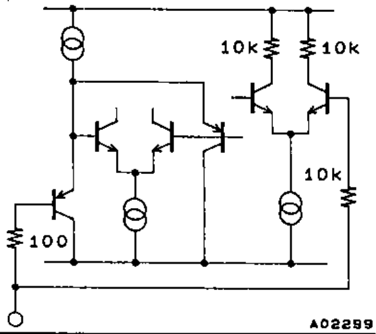
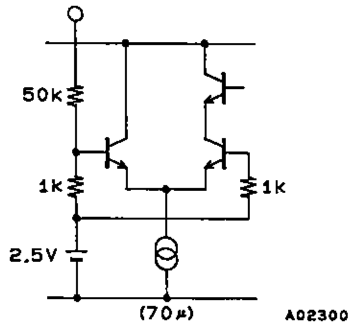
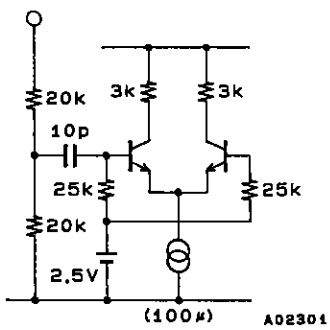
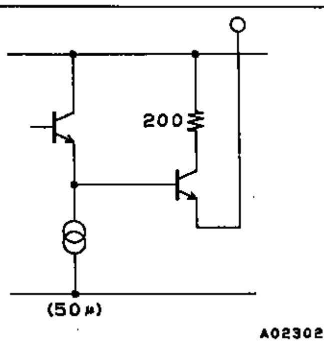
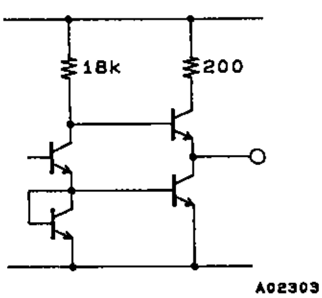
Unit (resistance: Ω, capacitance: F)

Pin No.	Symbol	Equivalent I/O circuit	Function
1	CHROMA-IN		This is the chroma signal input pin. It can handle burst signals (an unmodulated carrier for SECAM signals) with an amplitude of between about 50 and 800 mV p-p.
2	HPF. MONI		HPF output monitor This pin should be connected to V_{CC} in normal operation to avoid interference between pins 1 and 3.
3	FILTER		Phase comparator output The output is smoothed with a capacitor. The smoothed output level will be 2.0 V or lower for PAL, and 3.5 V or higher for SECAM or MESECAM.
4	GND		

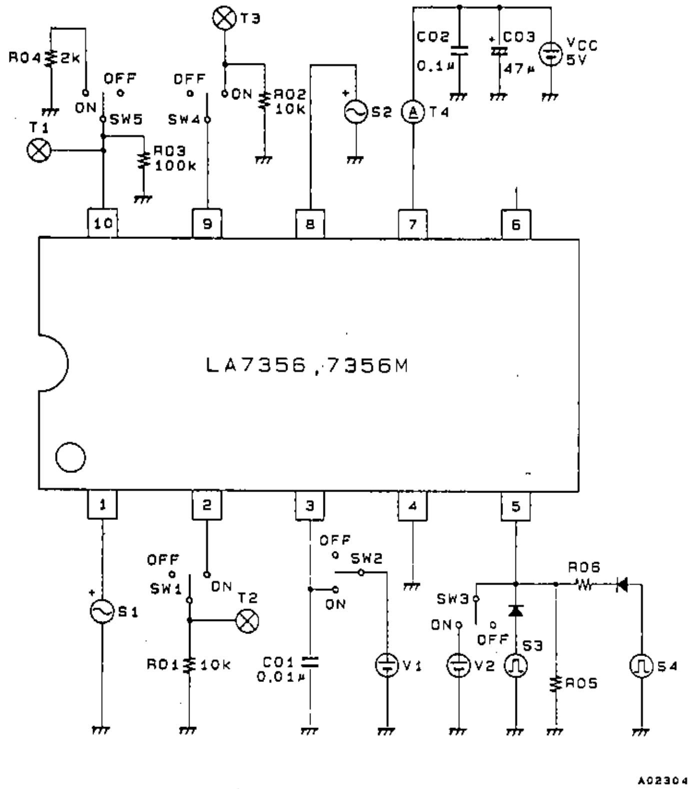
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Unit (resistance: Ω, capacitance: F)

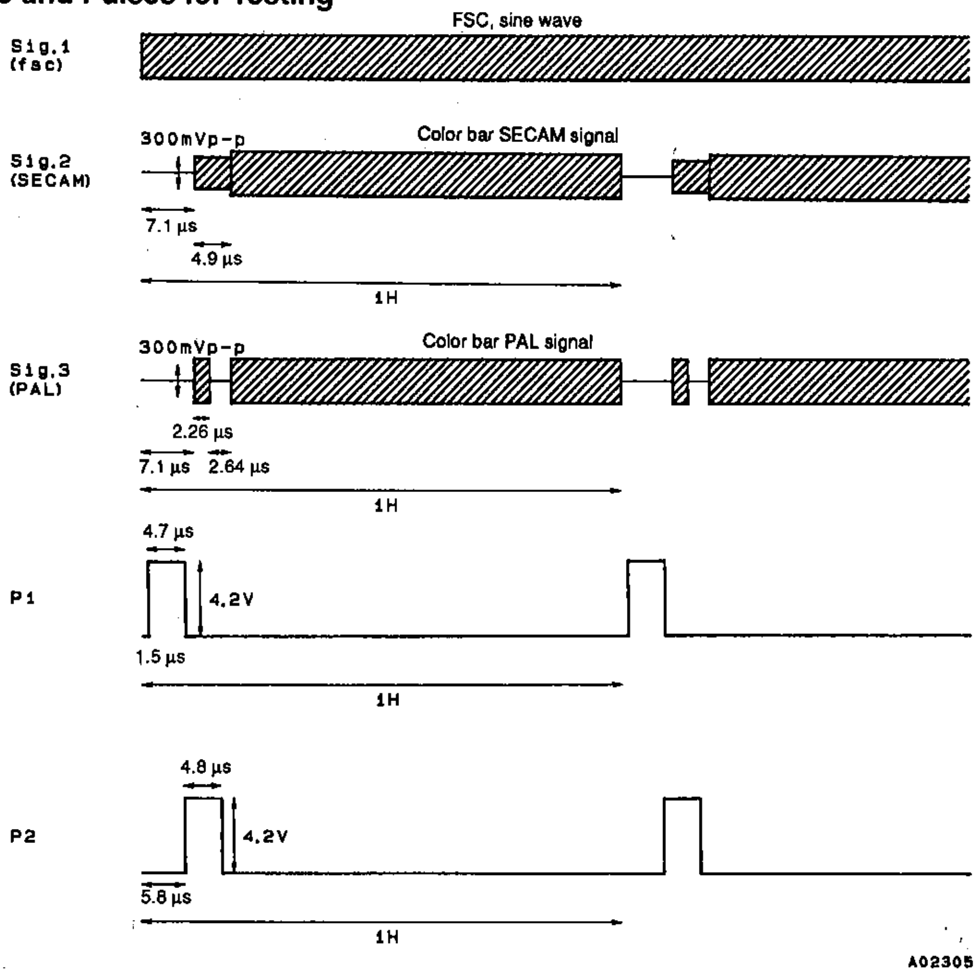
Pin No.	Symbol	Equivalent I/O circuit	Function
5	SYNC + BGP		Input for the BGP + SYNC signal The input level is 1.0 to 2.0 V during the SYNC period (⎍) and 3.0 to 4.5 V during the BGP period. Note that when used in conjunction with Sanyo LA7430 and LA7435 single-chip Y/C products, the external circuit connected to pin 5 is unnecessary since those single-chip circuits output a combined BGP and C.SYNC pulse (⎍).
6	DET-ADJ		Discrimination sensitivity adjustment Increasing the voltage applied to this pin shifts the discrimination toward PAL, and lowering that voltage shifts it towards SECAM. This pin is normally left open.
7	V_{CC}		
8	FSC-IN		This is the PAL fsc (4.43 MHz) input pin. It can handle amplitudes between about 300 and 800 mVp-p.
9	APF. MONI		APF output monitor This pin should be connected to V_{CC} in normal operation to avoid interference between pins 8 and 10.
10	DET-OUT		Discriminator output This pin outputs a high level (4.2 V) during SECAM or MESECAM, and a low level (about 0 V) during PAL.

Test Circuit Diagram

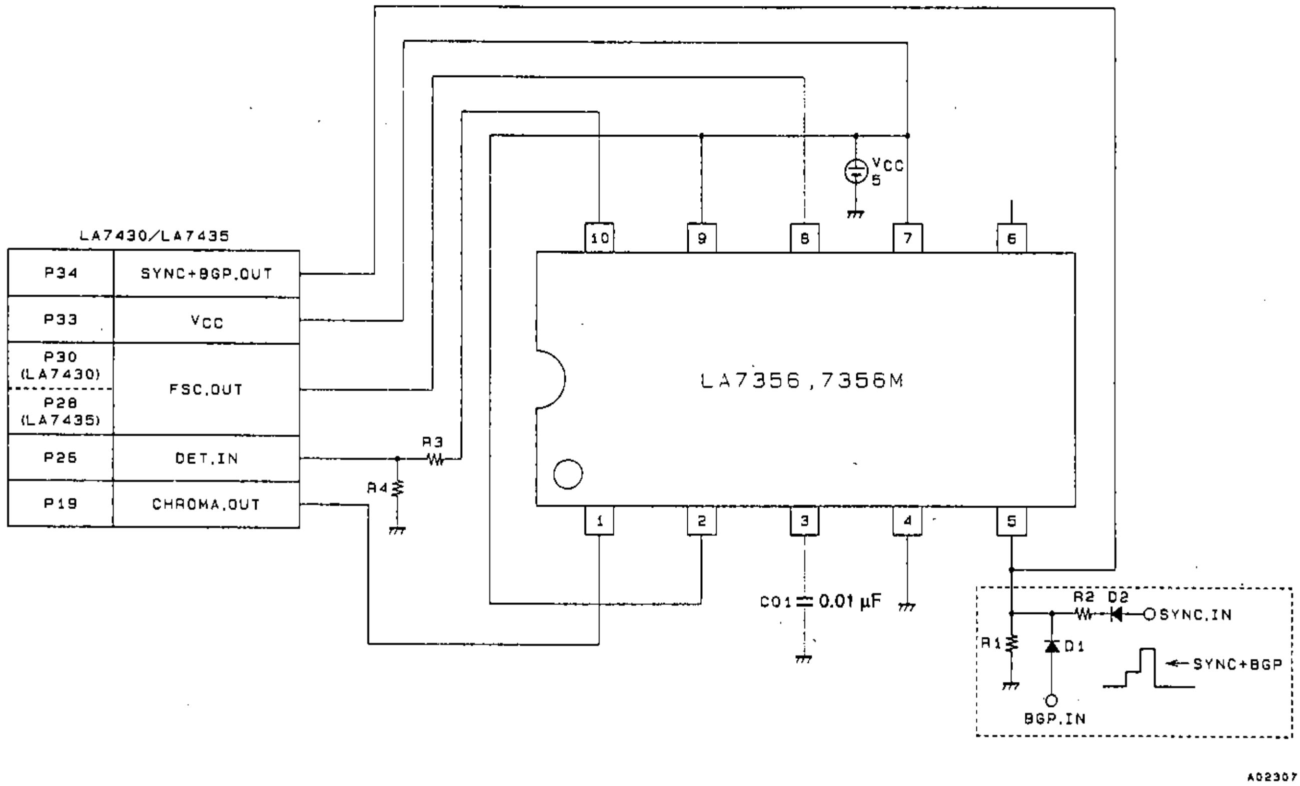


Unit (resistance: Ω, capacitance: F)

Input Signals and Pulses for Testing



Application Circuit Diagram



Application

Input the chroma signal to pin 1 and the PAL f_{SC} to pin 8. Also, input a signal that is the combination of the BGP and C.SYNC signals to pin 5. The output will be a high level during SECAM or MESECAM and a low level during PAL.

The output can be forcibly set to SECAM by connecting pin 3 to V_{CC} or forcibly set to PAL by connecting pin 3 to GND. This can be used to prevent incorrect operation during weak signal reception.

Note that when used in conjunction with Sanyo LA7430 (multi) and LA7435 (PAL/MESECAM) products, the external circuit connected to pin 5 is unnecessary since those products output a combined BGP and C.SYNC pulse.